九齊科技股份有限公司

Nyquest Technology Co., Ltd.

DATA SHEET

NY9UP64A *(OTP for NY9UxxxB)*

Universal Remote Controller with16 I/O

Version 1.1

Aug. 25, 2016

Revision History

Version	*Date*	*Description*	*Modified Page*
1.0	2016/2/25	Formal release.	-
1.1	2016/8/25	Adjust LVD option from 2.3v/2.4v to 2.2v/2.3v. Add note: PC0~2 of SOP16 package must be connected.	3, 4. 5

1. 概述

NY9UP64A 產品爲多功能遙控器的4位元微控制器，為嵌入式EPROM架構的OTP IC (One Time Programmable)，支援 NY9UxxxB MaskROM 產品。NY9UP64A有16根I/O並支援T-type按鍵矩陣。大灌電流的紅外線端口可以無需外加電晶體即能完成發射與接收功能。使用RISC精簡指令集架構，共有38條指令，可以很方便地以程式控制來完成不同的應用。提供待機模式(Halt mode)，可大幅度延長電池壽命。

2. 功能

- 工作電壓範圍： 2.0V ~ 3.6V。
- 4-bit RISC 精簡指令集架構的微控制器，共有38條指令。
- 64Kx10-bit ROM。
- 448x4-bit RAM，分成8頁，每頁56x4-bit。
- 1MHz 或 2MHz指令頻率。
- 提供待機模式(Halt mode)，可節省功耗，靜態電流(Isb)小於1uA @3.0V，斷電後電流小於0.1uA @1.3V。
- 在2.0V ~ 3.6V工作電壓與-20°C ~ +70°C的環境下，具有精準的+/-1.5%內阻震盪。
- 提供低壓復位(LVR=1.8V)、看門狗計時(WDT)、I/O復位功能(External Reset)。
- 2.2V 或 2.3V LVD flag 低電壓偵測。
- 一個中斷輸入可連結到一組獨立的堆棧(Stack)，並有多種中斷來源可以使用。
- 16根彈性的I/O腳。
  - 12根I/O (PAx, PBx, PCx) 為光罩選擇，可設定爲 initial output high, initial output low, bi-direction I/O with pull-high, bi-direction I/O without pull-high, initial pull-high input 或 initial floating input.
  - 4根I/O (PDx) 為暫存器控制，可設定為 bi-direction I/O 或 GPIO。
- 支援M-type、T-type或混合型態的按鍵喚醒。
- 紅外線端口提供 TX 和 RX應用，TX可選配大電流紅外線載波輸出。
- 12位元的可讀計時器可以選擇時鐘源，提供給IR的TX載波頻率與RX學習型計數器使用。
- 提供特殊的快速燒錄模式，以加快OTP燒錄時間。
- 支援特殊的ICP (In Circuit Programming) 燒錄功能，以方便客戶先組裝PCBA模組再進行燒錄。
- 提供可程式的Code資料保護模式。*(當Security-Bit 被燒斷後，資料將無法讀取。)*
- 提供多種出貨型態，以滿足客戶不同的應用需求。

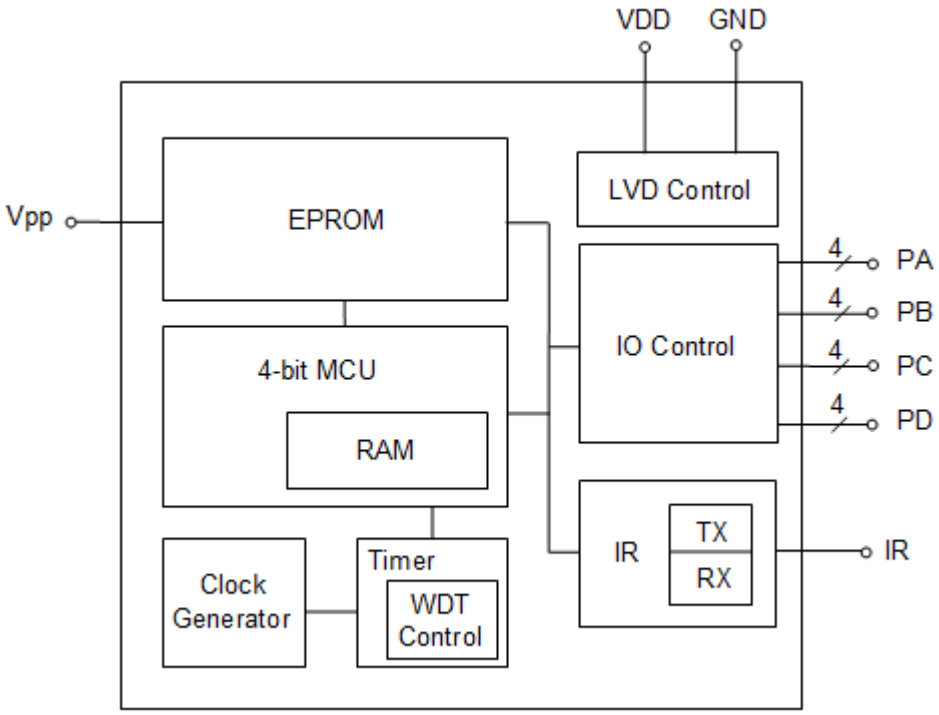
1. GENERAL DESCRIPTION

The NY9UP64A is a powerful 4-bit MCU with remote controller. It's embedded EPROM architecture, and the OTP (One Time Programmable) IC is designed to support NY9UxxxB MaskROM products. It has 16 I/O ports and supports T-type key matrix. One large sink current IR port can fulfill transmitting and receiving function without any bipolar transistor. The RISC MCU architecture is very easy to use, and various applications can be easily implemented. There are 38 instructions, and most of them are executed in single cycle. Furthermore, it provides the HALT mode (sleep mode) to extend battery life.

2. FEATURES

- Operating voltage range: 2.0V to 3.6V.
- 4-bit RISC type micro-controller with 38 instructions.
- 64Kx10-bit program ROM.
- 448x4-bit RAM, indirect RAM addressing mode is supported.
- 1MHz or 2MHz instruction frequency.
- HALT mode to save power, standby current <1uA @3V, battery-off current <0.1uA @1.3V.
- Precisely embedded oscillator with build-in resistor, +/- 1.5% deviation in 2.0V~3.6V and -20°C~+70°C.
- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.
- 2.2V or 2.3V LVD flag for low battery detection.
- One entrance for interrupt operation with an independent stack, multiple interrupt sources.
- 16 flexible I/Os.
  - 12 I/Os of PAx, PBx and PCx with optional function: initial output high, initial output low, bi-direction I/O with pull-high, bi-direction I/O without pull-high, initial pull-high input or initial floating input. *(Mask option)*
  - 4 I/Os of PDx with register control function: bi-direction I/O or GPIO. *(Register option)*
- M-type, T-type or mixed type key wakeup supported.
- Infrared port provides TX and RX application, optioned with large current IR carrier output for TX.
- 12-bit readable timer with selectable timer clock source for IR TX carrier frequency and RX learning counter.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP *(In Circuit Programming)* writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*
- Various shipping type for different application requirement.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

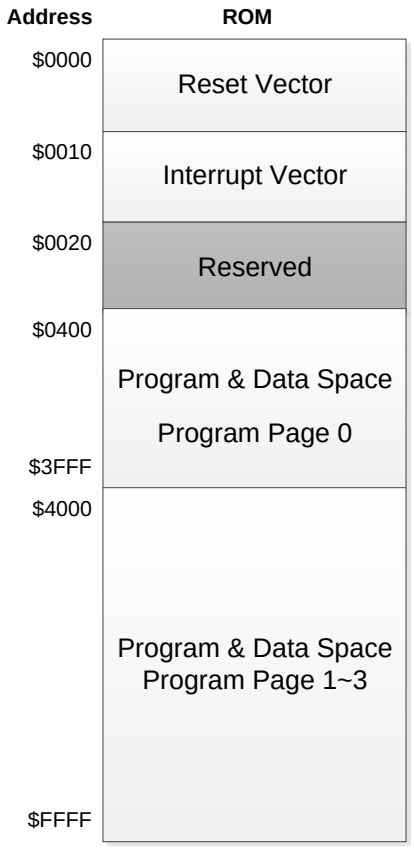
Pad Name	ATTR.	Description
Vpp	Power	Positive high power for programming.
VDD	Power	Positive power.
GND	Power	Negative power.
IR	I/O	Infrared port (TX & RX)
PA0/SDA	I/O	Bit 0 for Port A, or serial data input at programming mode.
PA1/SCL	I/O	Bit 1 for Port A, or serial clock input at programming mode.
PA2/Mode	I/O	Bit 2 for Port A, or select programming mode.
PA3/Vpp	I/O	Bit 3 for Port A, or positive high power for programming.
PB0~3	I/O	Bit 0~3 for Port B.
PC0~3	I/O	Bit 0~3 for Port C. *(PC0~2 must be set as high or low to avoid leakage current in SOP16 package.)*
PD0~3	I/O	Bit 0~3 for Port D.

5. MEMORY ORGANIZATION

The NY9UP64A has 64K words ROM, 448 nibbles of RAM and 21 nibbles of dedicated system control register. The registers are divided into 14 nibbles of system registers and 7 nibbles of memory registers. Besides, there are several registers without address allocation, and they can only be accessed by the special instructions such as clock source register (TCS) and timer register (TM).

5.1 ROM

A program data single ROM is provided and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 14-bit length address of ROM, the program page size is 16K words.



5.2 RAM

NY9UP64A provides 8 pages, and each page of RAM contains 56 nibbles. The page number (PG) register of RAM is defined by system register $0 for NY9U series, and its initial value is 0. Because the memory space is shared with the memory registers (address=0x00~0x07), the address for RAM is 0x08~0x3F.

6. INTERNAL OSCILLATOR

The system clock is 1MHz or 2MHz which is fast enough for most of applications. The clock generator is a Ring oscillator, and users can only select the internal resistor oscillation (INT-R). The INT-R oscillator accuracy is up to ± 0.5%, and the deviation is ± 1.5% in the full range of 2.0V~3.6V VDD and -20°C~+70°C temperature.

7. SYSTEM RESET

7.1 System Power-On & Power-Down

After Power-on, the power-on reset initialization will automatically be set out. The system takes 16ms to leave from the reset initialization procedure, and enters the normal operation and the program counter (PC) will start at the reset vector to execute the desired program.

7.1 LVR & LVD

When the system enters the normal operation, the power voltage must be kept in an effective working range. If the voltage is lower than the effective working voltage range, the system will work improperly.

To prevent the system crash, NY9U series supplies Low Voltage Reset (LVR) detectors. Once the LVR detector detects a harmful low voltage supply, it will cause a low voltage reset. The so-called “low voltage reset” point of the NY9U series IC is about 1.8V. The Low Voltage Detection (LVD) is an advanced detection of supply voltage. The LVD flag is read only and will be set to “0” if the supply voltage is lower than V_{LVD}; otherwise, set to “1”.

7.1 WDT

To recover from program malfunction, the NY9U series IC supports an embedded watch-dog timer reset. The WDTR function always works with the program executing. Users have to clear the WDT periodically to prevent from timing up with a reset generation. Typically, the minimum time-up period of the WDT is about 0.45s. Users can move a 0xE value to the INT system register to clear WDT.

8. I/O PORTS

There are 16 I/O ports, designated as PAx through PDx, and x=0~3. PAx, PBx, PCx ports can be configured by option code and I/O register, but the option code is fixed, and users can set I/O functions by I/O registers. The I/O ports PAx, PBx, PCx can be configured as six statuses, initial output high, initial output low, I/O (bi-direction) with pull-high, I/O (bi-direction) without pull-high, initial pull-high input or initial floating input by option. And when the chip is running, the status can be changed by I/O register control.

The table below shows the relation between them. (PX means PA, PB, PC register)

Category	Option	PX register write 1	PX register write 0
PXx (X=A~C, x=0~3)	initial output high	output high	output low
	initial output low	output high	output low
	I/O with pull-high	input with pull-high	output low
	I/O without pull-high (open drain)	Input floating	output low
	initial pull-high input	input with pull-high	input floating
	initial floating input	input with pull-high	input floating

Note: The PX0 & PX1 options have to be same, and the PX2 & PX3 options have to be same too.

The PD is different with PA, PB and PC, and it’ can’t be optional. The status of PD is I/O with pull-high initially, and the PD can be controlled more flexible by three registers (PD, PDDIR and PDATT) of system registers.

The pull-high resistor of all the I/O ports is about 125KΩ @3V for key matrix function usually.

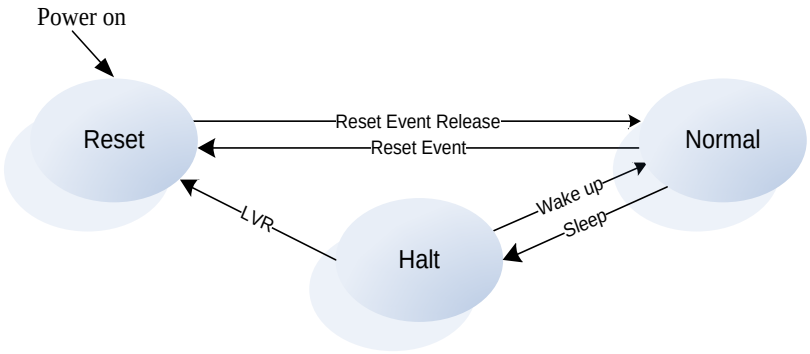
9. IR TX/RX

The NY9U series provides an independent pin (IR) for infrared transmit/receiver block, which is used to send or receive infrared signal. For the function of transmitter, users can set a variety of IR carrier frequency by the given clock source (TCS), DTHN, DTLN and the given value of 12-bit IR timer register (TM). As for the detailed

calculation of IR carrier frequency and applications, IR control register. For the receiver, the external BJT is no longer needed. Users can utilize the RXFF and RXRF interrupt mechanism through register TMC or read received data directly through IRRX[0] to apply for the desired program.

10. POWER SAVING MODE

The relationship between power saving mode, reset & normal mode is shown below.



10.1 Halt Mode

The system enters the halt mode if the HALT command executed. The halt mode is also known as the sleep mode. As implied by the name, the IC falls asleep and the system clock is completely turned off, so all the IC functions are halted and it minimizes the power consumption.

The only way to wake-up the sleeping system is an input port wake-up. The IC keeps monitoring the input pads during the halt mode. If the input status of any input pad changes to low, the system will be woken-up. Then the succeeding instructions after the HALT instruction will be executed after the wake-up stable time (about 60us). So before executing the HALT instruction, users have to keep in mind that the input port status is high.

If the IC is waked-up from the halt mode by the occurrence of LVR, it goes into the reset procedure.

10.2 T-type Scan Mode

In T-type scanning application, each port (PA~PD) can be selected as scan key independently by option PXx (X=A~D, x=0~3). It works as input with pull-high resistor and output fixed frequency low pulse in halt mode. Any of the keys touch would cause system wake-up.

Meanwhile, the frequency of key scan can be adjusted by option codes, such as about 15.625Hz, 31.25Hz, 62.5Hz and 125Hz.

10.3 Battery Off

If the battery is off from IC, IC goes into ultra-low power consuming mode. And the status makes internal SRAM keep its data for over two hours until the new battery is on, with external 47uF capacitor.

11. ELECTRICAL CHARACTERISTICS

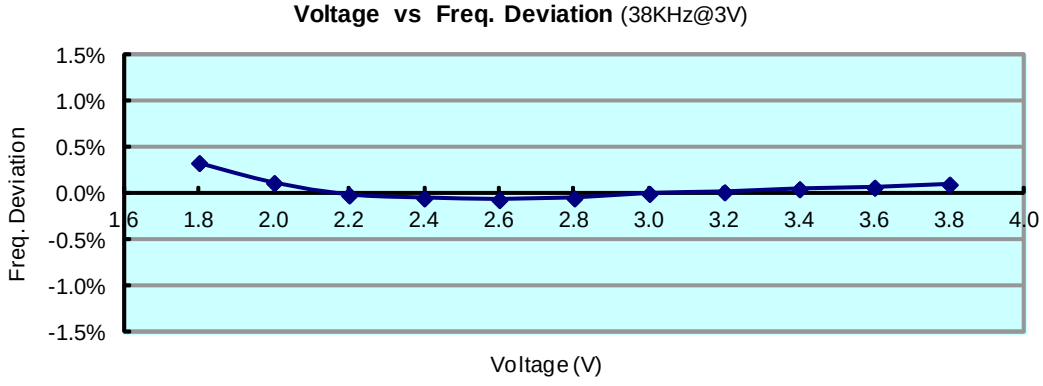
11.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
V_{DD} - V_{SS}	Supply voltage	-0.3 ~ +4.0	V
V_{IN}	Input voltage	V_{SS}-0.3V ~ V_{DD}+0.3	V
T_{OP}	Operating Temperature	-20 ~ +70	°C
T_{ST}	Storage Temperature	-40 ~ +85	°C

11.2 DC Characteristics *(V_{DD}=3.0V, T_A=25ºC, unless otherwise specified)*

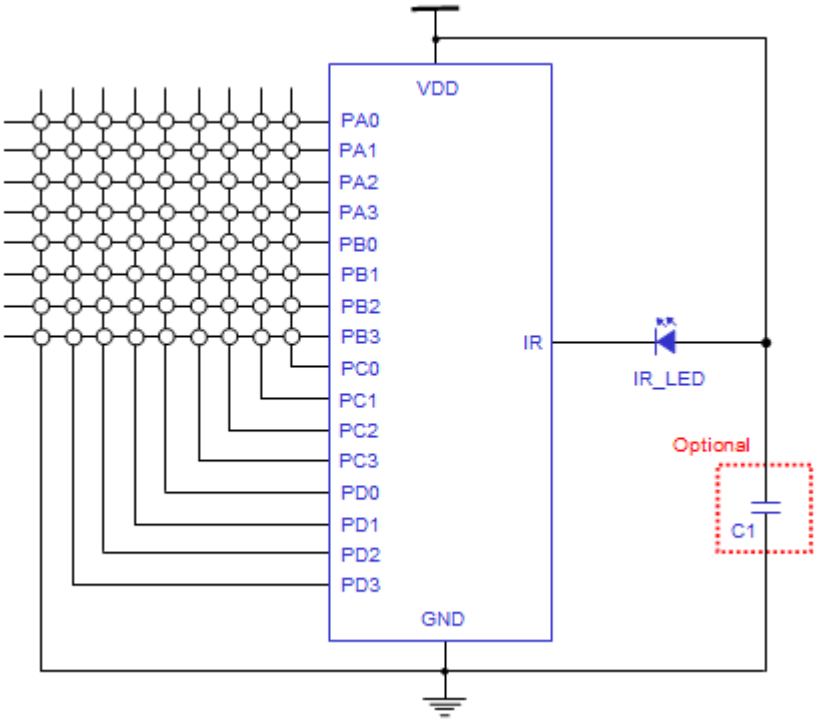
Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage		2.0	3	3.6	V	1 MHz & 2MHz
I_{SB}	Supply current	Halt mode			1	uA	Sleep, no load
I_{Scan}		Scan mode			2	uA	T-type key scan
I_{OP}		Operating mode		2.0		mA	1MHz, no load
				2.5		mA	2MHz, no load
V_{IH}	Input high level			0.7*V_{DD}		V	
V_{IL}	Input low level			0.5*V_{DD}		V	
I_{IL}	Input current (Internal 125KΩ pull-high)			24		uA	V_{IL} = 0V
I_{OH}	Output high current			-9		mA	V_{OH} = 2.0V
I_{OL}	Output low current			18		mA	V_{OL} = 1.0V
I_{IR}	IR sink current			350		mA	V_{IR} = 1.5V
D_{CAP}	IR capture distance			15		cm	
△F/F	Internal OSC frequency deviation		-1.5		1.5	%	V_{DD}: 2.0V ~ 3.6V, Temp: -20°C ~ +70°C

11.3 Voltage vs. Frequency

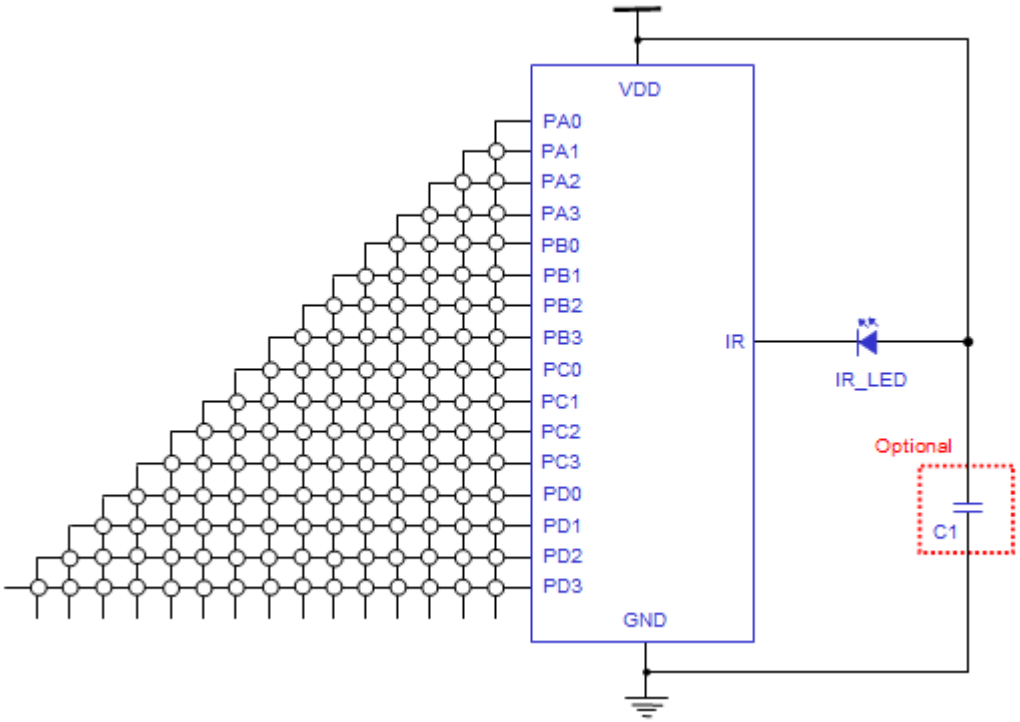


12. APPLICATION

(1) M-type Key Scan Keyboard (Matrix)

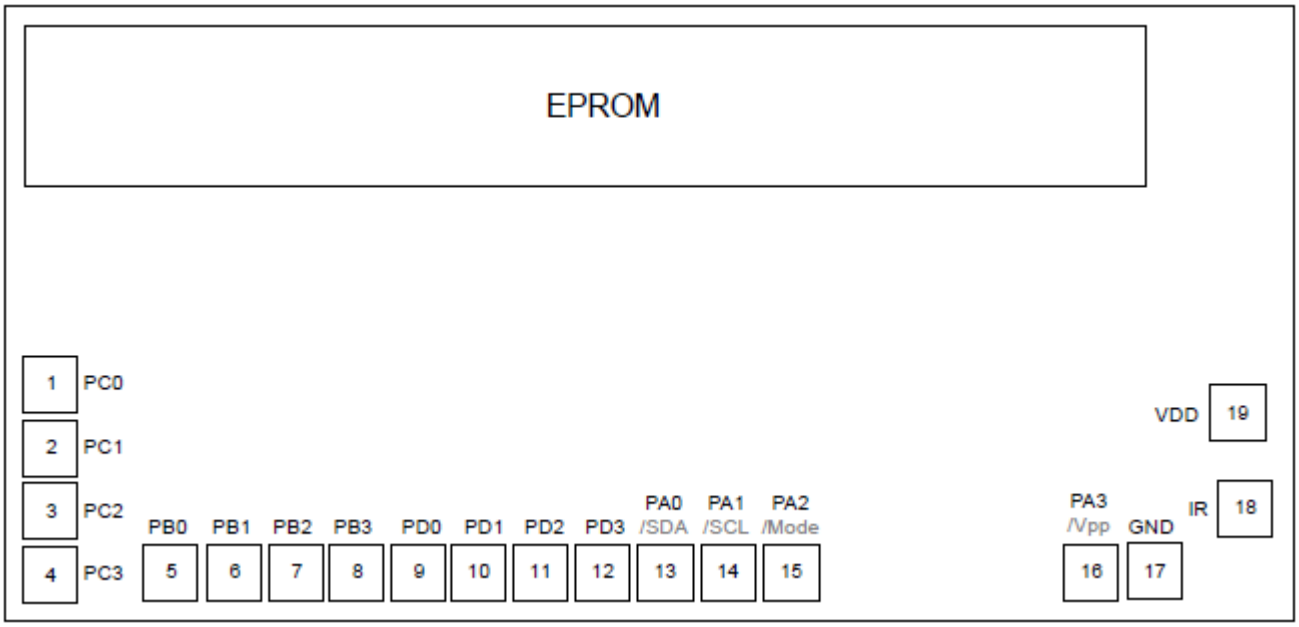


(2) T-type Key Scan Keyboard (T-Scan)



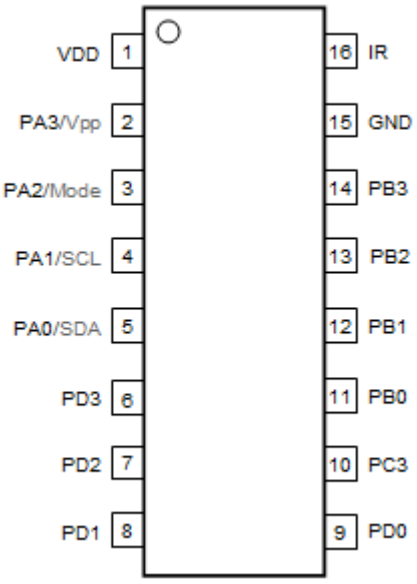
Note: C1 is a power saving cap to keep the code data in case users replace the battery.

13. DIE PAD DIAGRAM



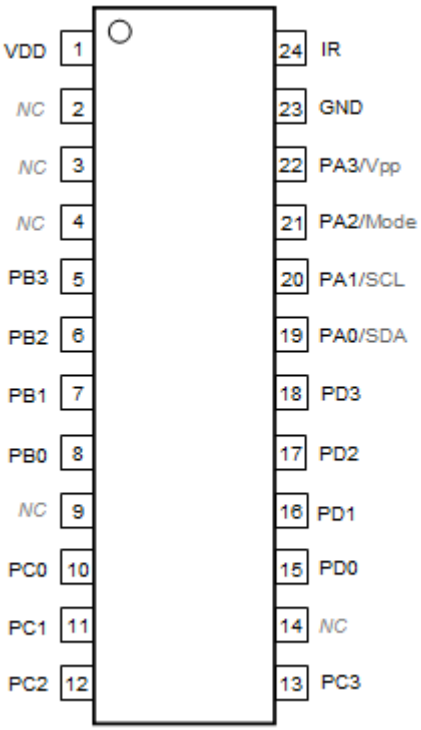
14. PACKAGE PIN ASSIGNMENT

16-pin SOP (150mil)



NY9UP64AS16

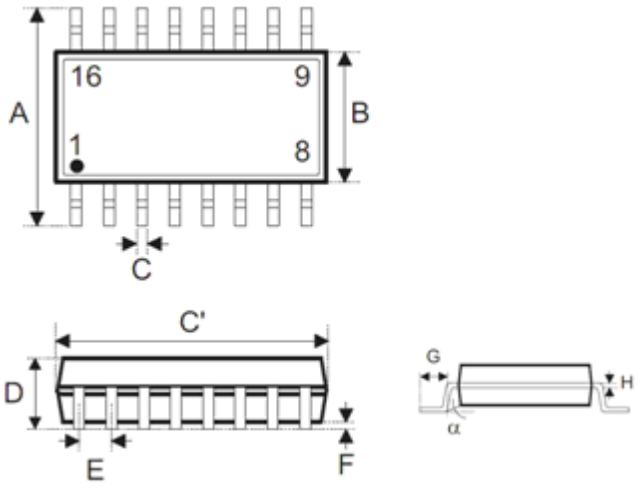
24-pin SSOP (150mil)



NY9UP64AU24

15. PACKAGE DIMENSION

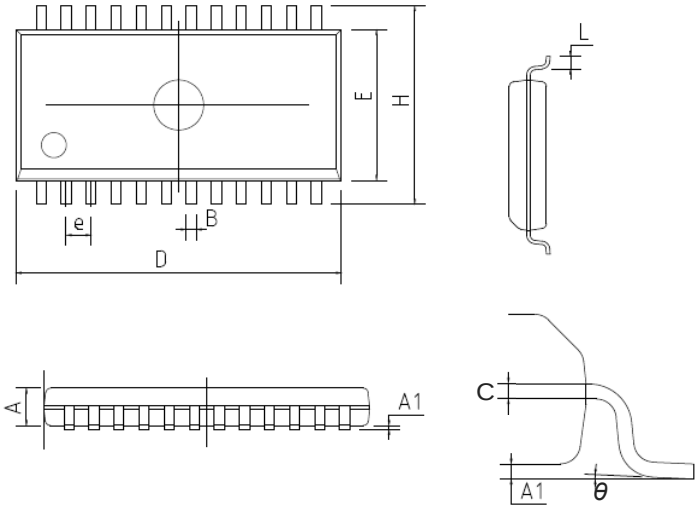
15.1 16-Pin Plastic SOP (150 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A		0.236 BSC			6.00 BSC	
B		0.154 BSC			3.90 BSC	
C	0.012	-	0.020	0.31	-	0.51
C'		0.390 BSC			9.90 BSC	
D	0.065	-	0.069	1.64	-	1.75
E		0.050 BSC			1.27 BSC	
F	0.004	-	0.010	0.10	-	0.25
G	0.016	-	0.050	0.40	-	1.27
H	0.004	-	0.010	0.10	-	0.25
α	-	-	8°	-	-	8°

Note: For 16-pin SOP, 50 units per tube.

15.2 24-Pin Plastic 0.635-SSOP (150 mil, Lead pitch 0.635mm)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.049	-	0.061	1.25	-	1.55
A1	0.002	-	0.010	0.05	-	0.25
B	0.008	-	0.012	0.19	-	0.31
C	0.006	-	0.010	0.15	-	0.25
D	0.337	-	0.344	8.55	-	8.75
e		0.025 BSC			0.635 BSC	
E	0.150	-	0.157	3.80	-	4.00
H	0.224	-	0.248	5.70	-	6.30
L	0.012	-	0.035	0.30	-	0.90
θ	0°	-	7°	0°	-	7°

Note: For 24-pin SSOP, 50 units per tube.

16. ORDERING INFORMATION

P/N	*Shipping Type*	*Remarks*
NY9UP64A	Die	Empty ROM data
NY9UP64A -xxxx *1	Die	Programmed ROM data
NY9UP64AW-xxxx *1	Wafer	Programmed ROM data
NY9UP64AS16	SOP-16	Width 150 mil
NY9UP64AU24	0.635-SSOP-24	Width 150 mil, Pin Pitch 0.635mm

**1 "xxxx": Code number*